REMARKS

In the patent application, claims 1-31 are pending. In the final office action, all pending claims are rejected.

Applicant has amended claims 1, 3, 6, 13, 18, 19, 22, and 31, and added new claims 32 through 35.

Claims 1 and 22 have been amended to move some of the claim language in the preamble to the characteristic part. Claim 3 has been amended to correct for a typographical error. Claim 6 has been amended to clarify where the host module is located. Claim 13 has been amended to remove some of the claim language in the preamble. Claim 18 has been amended to replace "PDA" with "personal data assistant device". Claim 19 has been amended to remove the acronym "CS". Claim 31 has been amended mainly to remove "(SPI)" and "(CS)".

The changes are of formal matters. No new matter has been introduced.

The support for new claim 32 can be found in Figure 4.

The support for new claim 33 can be found in claim 2.

The support for new claims 34 and 35 can be found in Figure 4, where the further signal generating means is depicted as the master part, and the causing means is depicted as the sub-bus system.

At section 4, claims 1-31 are rejected under 35 U.S.C. 102(e) as being anticipated by *Moro* (U.S. Publication No. 2003/0056050) in view of *Iida et al.* (U.S. Patent No. 2004/01566242, hereafter referred to as *Iida*). The Examiner states that *Moro* discloses a method for enhancing performance of a memory card by operating SPI or SD-1 mode so that there are N-M unused data lines.

The Examiner further states that *Moro* discloses providing in the memory device for generating at least one further signal (see Figure 6, paragraphs 0055-0057).

The Examiner admits that *Moro* does not specifically disclose the step of causing to exchange data between the host module and the memory device using at least one of the unused data lines, but points to *Iida* for disclosing such data exchange (figure 2, table 2, paragraphs 0041-0045).

It is respectfully submitted that *Moro* discloses using one host device to exchange data with two SD cards wherein data lines DAT0-DTA4 can be used for different modes as shown in Figure 5. However, *Moro* does not disclose providing in the memory device for generating at least one further signal. As described in paragraphs [0055] and [0057], the command signals are sent from the host controller 111 to the individual memory cards.

In contrast, the further signal is generated in a module in the memory device in the claimed invention.

In sum, *Moro* does not disclose "causing an exchange of data, using at least one of the unused data lines" even in SD 1-bit mode. *Moro* does not disclose generating a further signal in the memory device for causing data exchange on any unused data line based on at least one further signal.

In contrast, in the claimed invention, data is caused to exchange on at least one of the unused data lines due to the generation of at least one further signal in the memory device when the host module is operated in the data mode that has unused data lines.

Iida discloses a method of bus width switching for data transfer in a card type storage device. In the card type storage device, the data terminals are provided with pull-up resistors and the data terminals are connected to a level detection circuit. The detection circuit is used to detect whether one or more of the pull-up resistors are in the open condition so as to determine the bus width for data transfer (paragraph 0009). Thus, while *Iida* discloses a mode selection procedure wherein the conventional MMC mode, 1-bit high speed MMC mode, 4-bit high speed MMC mode or 8-bit high speed mode is selected for data transfer, *Iida* does not disclose the step of causing to exchange data between the host module and the memory device using at least one of the unused data lines.

The Examiner states that *Iida* teaches the use of unused data lines (DAT4-DAT7) to transfer data between the host interface and the memory device when the level detection circuit 221 determines the high-speed 8-bit MMC mode or 4-bit MMC mode (paragraph 0044-0048).

It is respectfully submitted that *Iida* uses the potential on data lines (DAT4 – DAT7) to indicate what mode is to be used. The potential on these data lines cannot be considered as data transfer for the following reasons:

First, this pattern of potential levels for mode indication exists before any data can be transferred because data transfer occurs only after the level detection circuit 221 determines what mode should be used based on the pattern. Thus, mode indication is not part of the data transfer.

Second, the pattern of potential levels exists only for mode indication purposes. Even if the detection of this pattern for mode selection can be considered as an exchange of data as alleged by the Examiner, this "exchange of data" is not based on a further signal generated by the module.

Third, the pattern of potential levels on the unused data lines for indicating a particular data mode is always the same anytime a memory device is used in a host interface. Otherwise the detection module cannot determine what mode is to be used based on the pattern. The pattern of potential levels on the unused data lines does not change after the data transfer is taken place on the used data lines. When the potential levels on the unused data lines do not change, there is no data exchanged on the unused data lines.

The purpose of data exchange is to provide new information after the data mode has been selected. For that reason, a further signal is generated in the memory device so as to cause data to be exchanged between the host device and the memory device using at least one of the unused data lines. It is impossible to convey new information without varying the potential levels on the unused data lines after the data mode has been determined. In *Iida*, there is no other data transmission between a card and a host after the data mode is selected.

In sum, *Moro* does not disclose generating a further signal in the memory device. *Iida* does not disclose generating a further signal in the memory device so as to cause an exchange of data based on the further signal using the unused data lines.

For the above reasons, *Iida* is irrelevant to the invention as claimed in claims 1, 13, 22, 27, 30, 32 and 34 and the combination of the teachings of *Moro* and *Iida* does not render the claimed invention as claimed in claims 1, 13, 22, 27, 30, 32 and 34 obvious.

As for claims 2, 4, 10, 15, 24 and 33, they are dependent from claim 1, 13, 22 and 30 and recite features not recited in claim 1, 13, 22 and 30. For reasons regarding claims 1, 13, 22 and

30 above, claims 2, 4, 10, 15, 24 and 33 are also distinguishable over the cited *Moro* and *Iida* references.

In rejecting claims 2, 15 and 24, the Examiner points to Figure 6 and paragraph 0055 of *Moro* for disclosing a command signal conveyed to the host module on another one of the unused data lines. It is respectfully submitted that, in Figure 6, the CMD pins in the host controller 111 are connected to the CMD pin of SD card #1 and that of SD card #2. The SD card is depicted in Figure 9, wherein command signals are conveyed through the CMD pin 125, not through any of the data lines DAT0-DAT3. Paragraph [0055] describes the pin assignment as depicted in Figure 5. In Figure 5, command and response signals are conveyed through the CMD pin, not through any unused data lines (DAT2 and DAT1 in SD Mode 1 bit and SPI Mode). *Moro* does not disclose using unused data lines to send a command signal to the host module as claimed in claims 2, 4, 10, 15, 24 and 33. Furthermore, the command signal is conveyed from the host controller 111 to the SD memory card (see paragraphs [0055] and [0057]). *Moro* does not disclose generating a further signal in the memory device.

In rejecting claims 4 and 10, the Examiner states that *Moro* discloses conveying a command signal on one of the unused data lines (Figure 2, paragraphs [0045]-[0049]).

It is respectfully submitted that Figure 2 shows four data pins DAT0-DAT3 and a command signal pin CMD. Paragraphs [0045]-[0047] and [0049] only describe the bi-directional buffer in the driver circuit for each data pin and how the lead-through current is prevented. Paragraph [0048] describes the bi-directional buffer in the driver circuit for the CMD pin. The Examiner fails to point out where in these paragraphs does *Moro* disclose conveying a command signal on one of the unused data lines. Furthermore, the command signal in *Moro* is conveyed from the host controller to the memory cards. This command signal has nothing to do with the further signal generated in the memory device.

For the above reasons, claims 2, 4, 10, 15, 24 and 33 are clearly distinguishable over the cited *Moro* and *Iida* references.

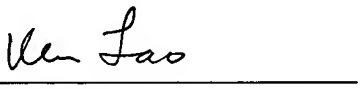
As for claims 3, 5, 11, 12 and 16, they are dependent from claims 2, 4, 10 and 15 and further dependent from claims 1 and 13, and recite features not recited in claims 1, 2, 4, 10, 13 and 15. For reasons regarding claims 1, 2, 4, 10, 13 and 15 above, claims 3, 5, 11, 12 and 16 are also distinguishable over the cited *Moro* and *Iida* references.

As for claims 6-9, 14, 17-21, 23, 25, 26, 28, 29, 31 and 35, they are dependent from claims 1, 13, 22, 27, 30, 32 and 34 and recite features not recited in claims 1, 13, 22, 27, 30, 32 and 34. For reasons regarding 1, 13, 22, 27, 30, 32 and 34 above, claims 6-9, 14, 17-21, 23, 25, 26, 28, 29, 31 and 35 are also distinguishable over the cited *Moro* and *Iida* references.

CONCLUSION

Claims 1-35 are allowable over the cited *Moro* and *Iida* references. Early allowance of all pending claims is earnestly solicited.

Respectfully submitted,



Kenneth Q. Lao
Attorney for the Applicant
Registration No. 40,061

WARE, FRESSOLA, VAN DER SLUYS
& ADOLPHSON LLP
Bradford Green, Building Five
755 Main Street, P.O. Box 224
Monroe, CT 06468
Telephone: (203) 261-1234
Facsimile: (203) 261-5676
USPTO Customer No. 004955